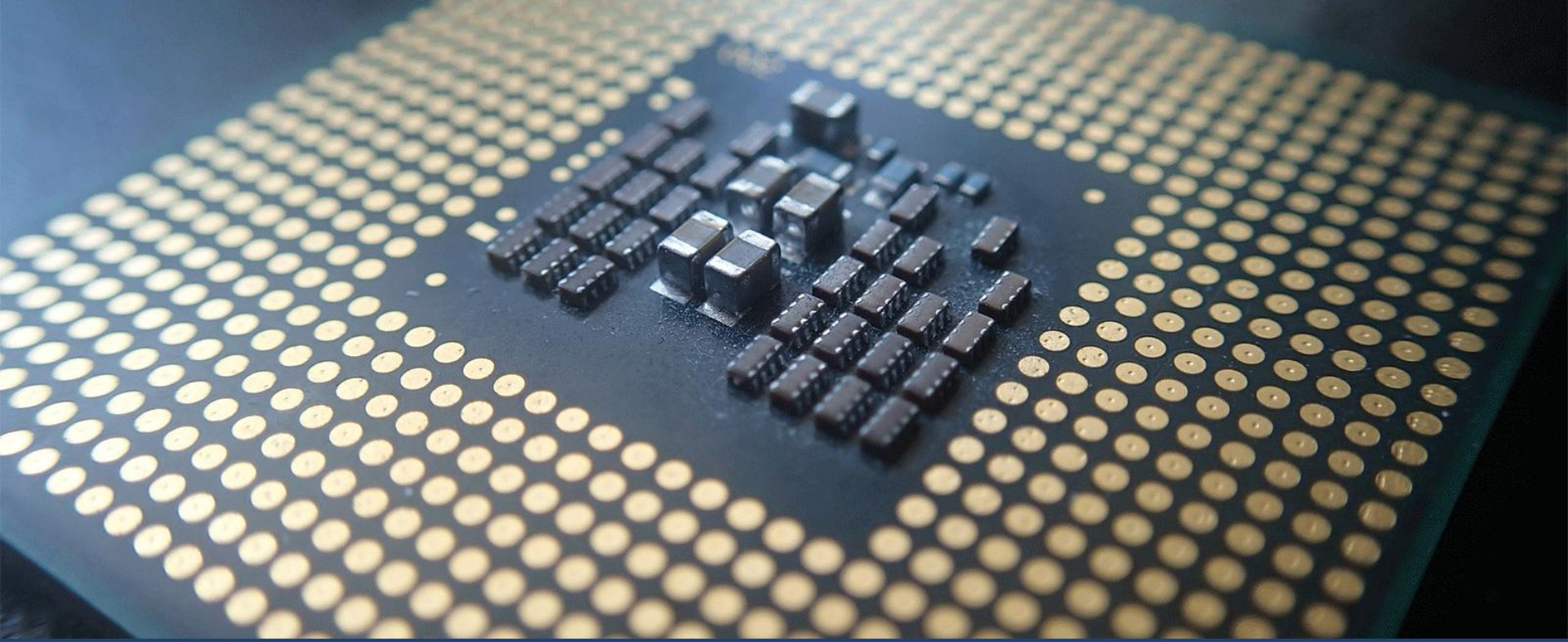
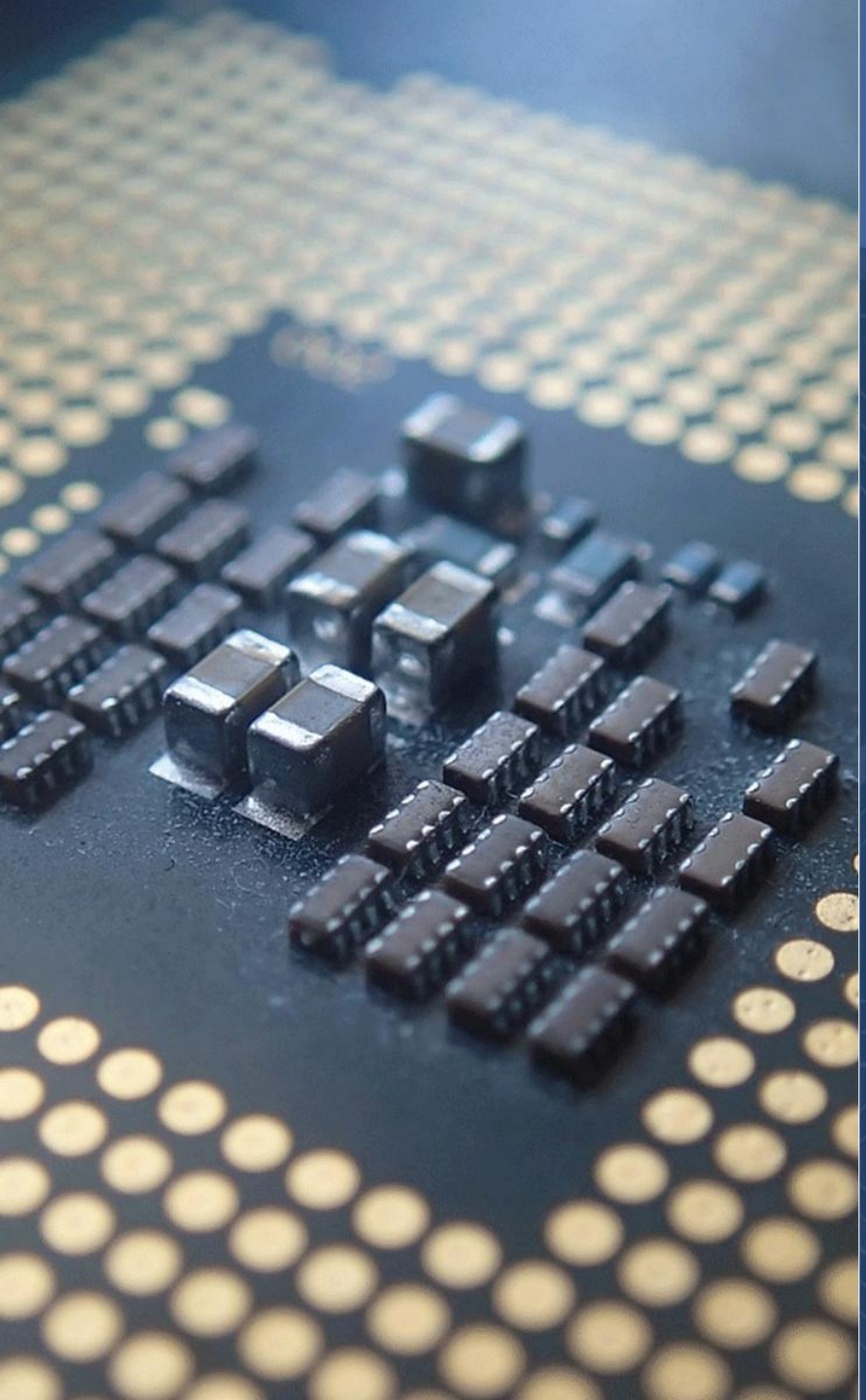


초미세 공정 한계 극복을 위한 반도체 공정 기술 개발의 최신 동향 및 미래

Latest Trends and Future of Semiconductor Process Technology Development for Overcoming the Limits of Ultra-Fine Processes

발표자: 정기창
장소: 전남대학교
일시: 2026년 5월 14일



CONTENTS

Kichang Jung

Education

- 전남대학교 공과대학 응용화학공학부 학사 (2011년)
- 전남대학교 공과대학 신화학소재공학과 석사 (2013년)

Research topic: GaN기반 LED 구조 개선을 통한 광 효율 개선 및 a-plane 결정을 갖는 GaN을 이용한 efficiency droop 문제해결

- University of California, Riverside PhD (2019년)

Research topic: Cu2O photocathode with faster charge transfer by fully reacted Cu seed layer to enhance performance of hydrogen evoluation in solar wafer splitting applications.

Experience

- 한국광기술원 학생연구원 (2010-2012년)
- 한국광기술원 위촉연구원 (2014년)
- Technology development process Engineer (2020-present)

- Intel Corporation
- Semiconductor manufacturer
- Founded: 1968
- Founders: Gordon Moore, Bobert Noyce, Arthur Rock
- Number of employees: 85,000
- Headquarters: Santa Clara, California, US

- Client Computing (CCG)
- Data Center and AI (DCAI)
- Network and Edge (NEX)
- Mobileye
- Intel Foundry Services (IFS)

Introduction

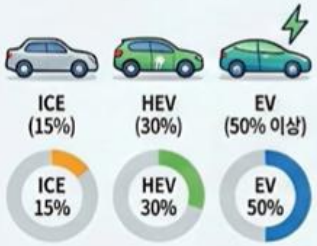
AI 시대, 반도체 산업의 대격변: 2030년 전망

자동차 산업의 대전환: 바퀴 달린 컴퓨터

전기화(EV)와 자율주행이 반도체 수요 견인

2030년, 전체 차량 관매리 약 50%가 전기처(HEV 포립)

엔진 유형에 따라 급증하는 전력 반도체 비중



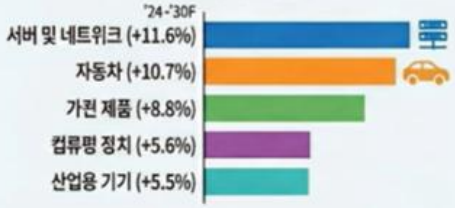
자율주행 레벨 상승 = 반도체 비용 10배 이상 증가

SDV(소프트웨어 정의 차량) 시대의 도래
소프트웨어 업데이트만으로 차량 기능 향상

고성능 SoC 및 AI 가속기 중요성 증가

글로벌 반도체 시장: 1조 달러 시대를 향하여

AI와 자동차가 미래 성장 주도



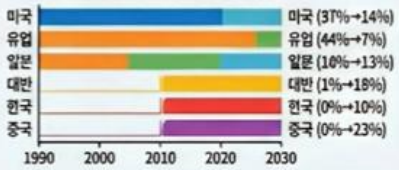
반도체 패권 경쟁: 공급망의 재편

지역별 본업화 심화: 설계는 미국, 제조는 아시아

2030년까지 1.5조 달러 이상의 Fab 투자 골드러시

지난 20년긴의 투자 충액과 탖억는 규모

글로벌 W께 극퍼 이금의 시유



미·중 경쟁이 이끄는 공급망 현지화

미국 (CHIPS 법, 첨단 Fab 유치)

중국 (상속 굥청 중심 자급자륵)

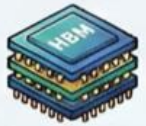
AI 혁명의 심장: 서버 및 네트워크

생성형 AI, 데이터센터 수요 폭발의 기폭제

2090년까지 전력 소비량 두 배 이상 층가 매족

데이터센터 첩 시장의 절반은 AI 가속기

HBM(고대역폭 메모리), AI 시대의 필수 부품



고성능 GPU 병목 해결

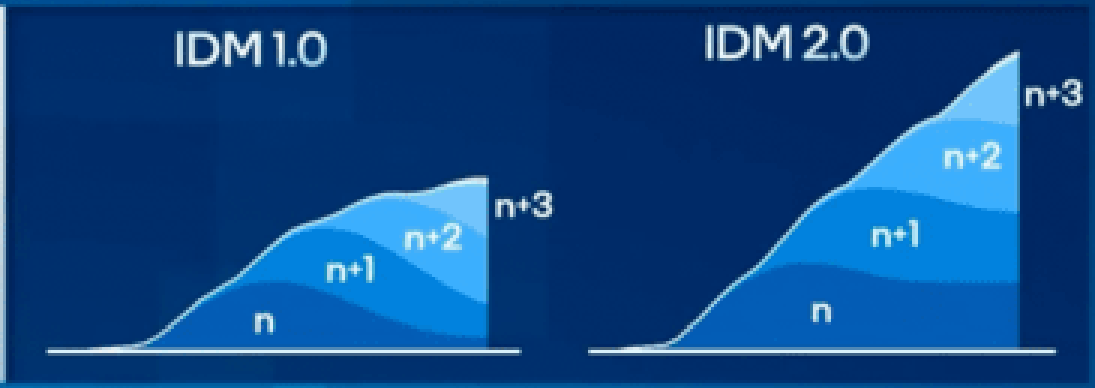
통신 시랑, GaN RF 첩으로의 전환 가속

Intel's Vision

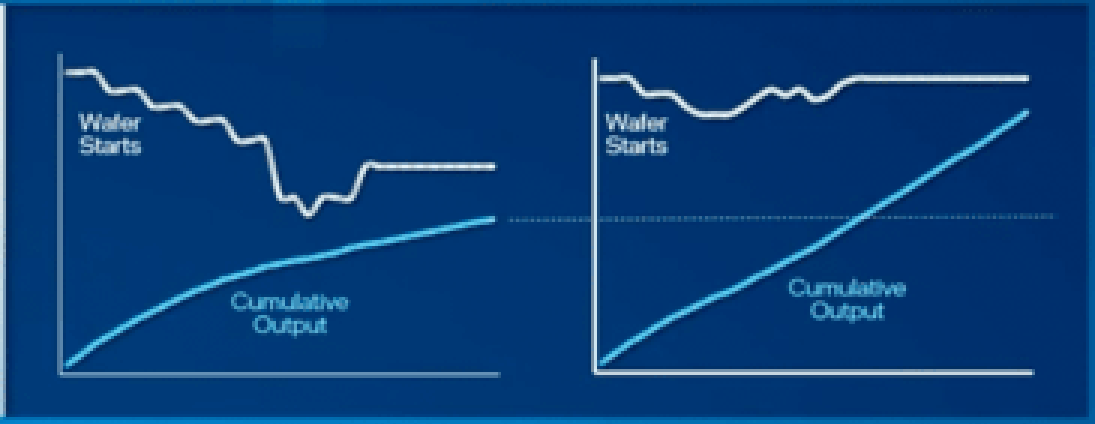
Being an IDM makes us better at IFS.....and

IFS makes us a better IDM

Using assets longer



Better Output from Assets

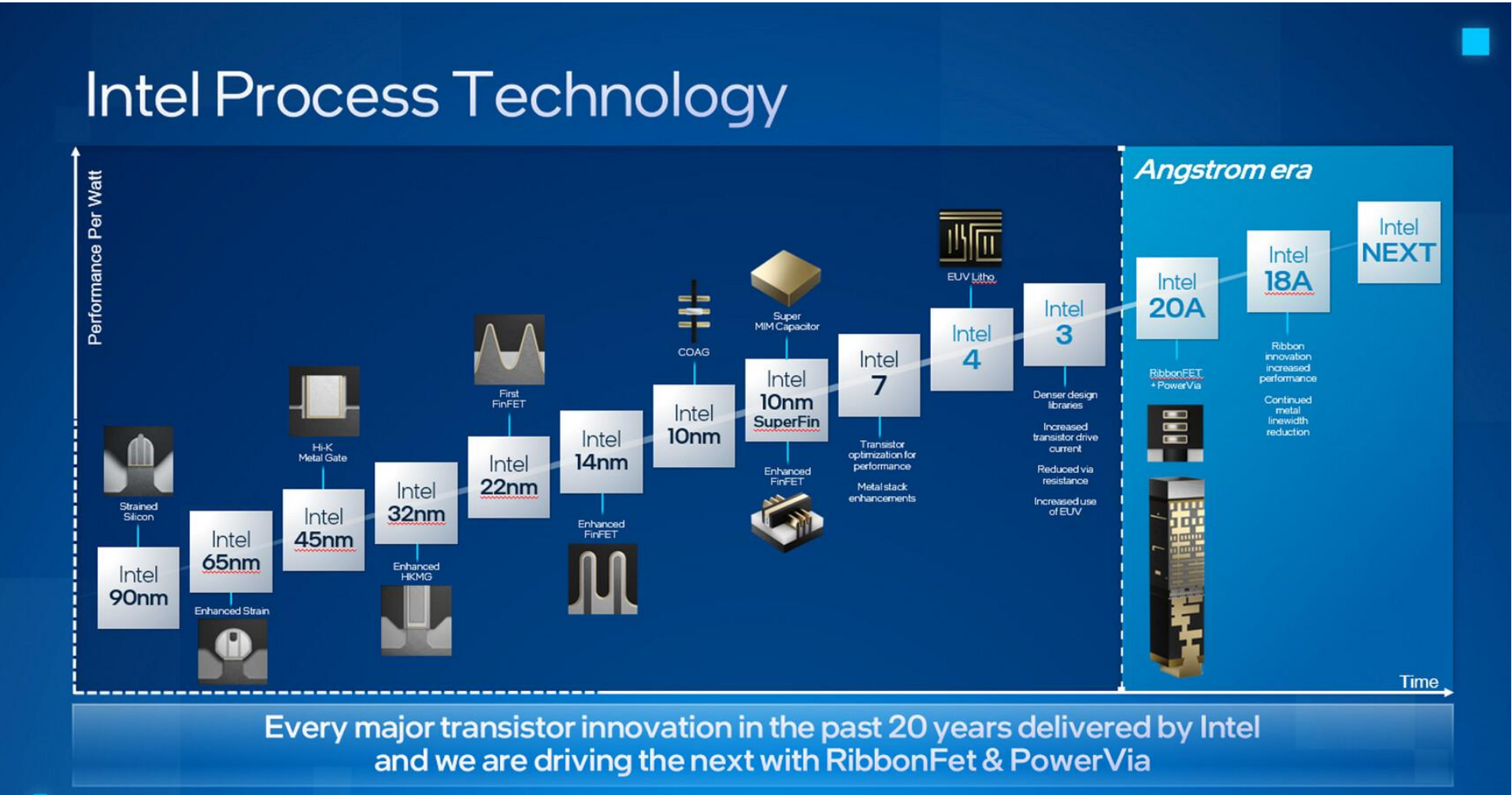


Manufacturing
Improved asset utilization
Economies of scale
Leverage R&D investment

IP & Architecture
Broader IP portfolio
Robust PDK and design ease-of-use

Customer Engagement
Co-innovation
Demanding customers requirements

Intel's Vision



 *Graphic is for illustrative purposes only and is not to scale

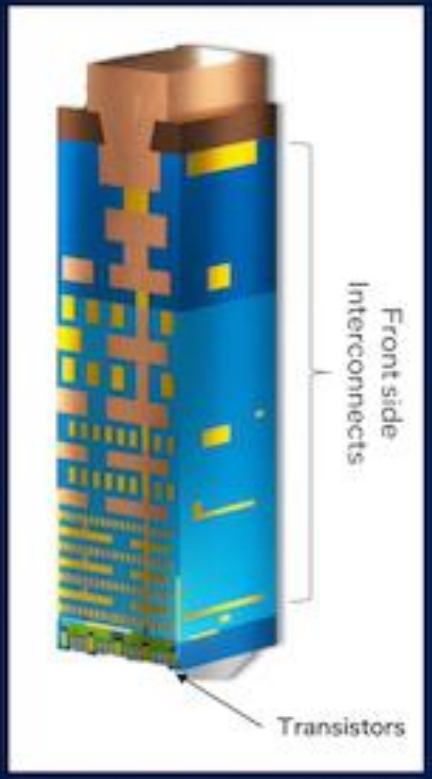
Intel's Vision

Frontside Power Delivery vs Backside Power Delivery

Frontside Power Delivery

Signal wires and power wires compete for the same resources at every metal layer.

Requires aggressive scaling of metal layer pitches:
- High cost
- Higher voltage droop
- Higher RC delay

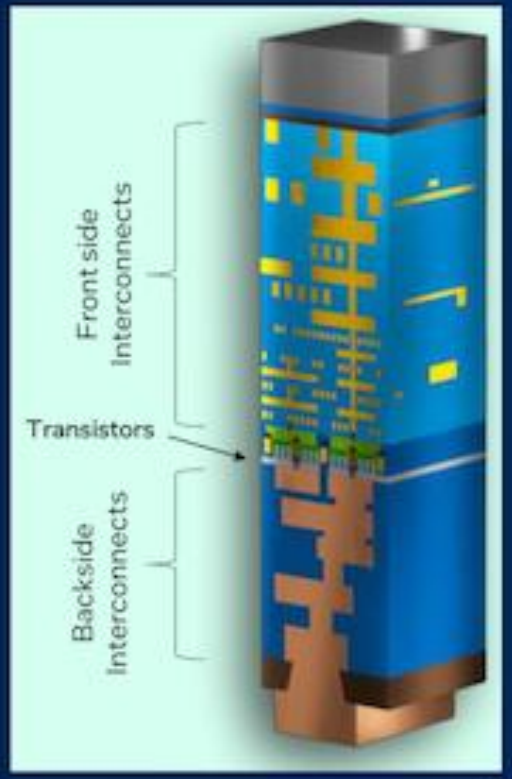


Backside Power Delivery

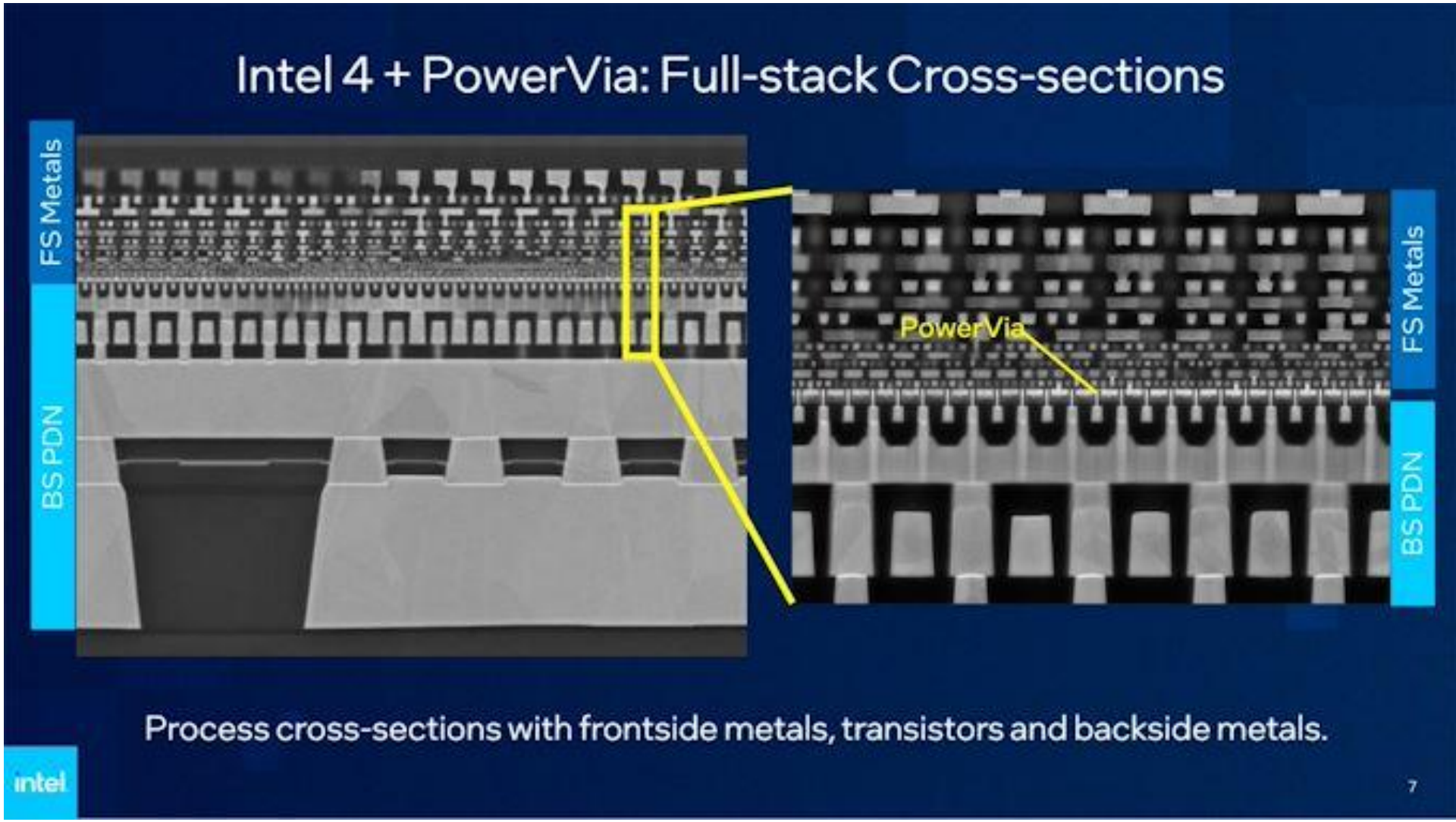
Signal wires and power wires are decoupled and optimized separately.

Value Proposition
- Higher Performance
- Lower Cost

Risks:
- Yield
- Reliability
- Thermal Dissipation
- Debug Capability



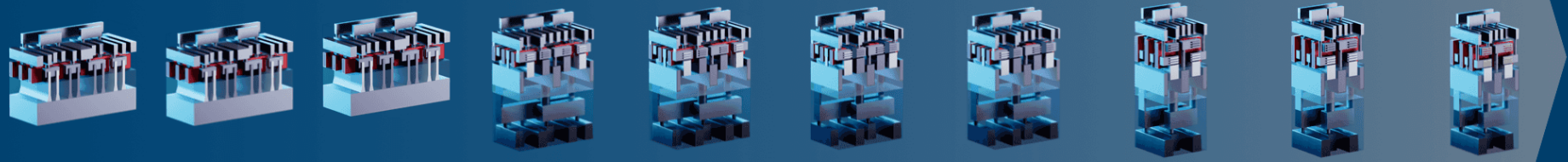
Intel's vision



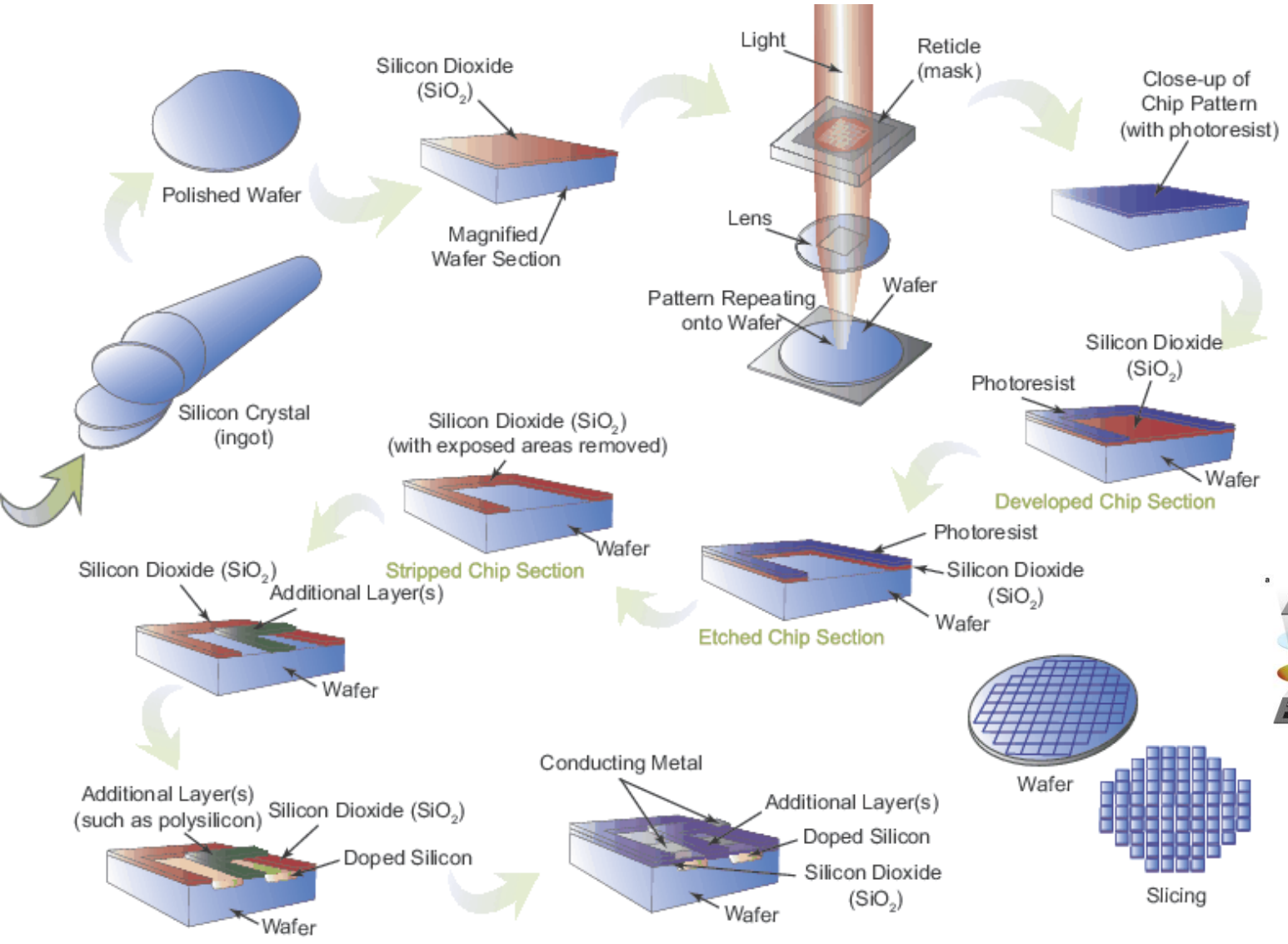
Introduction

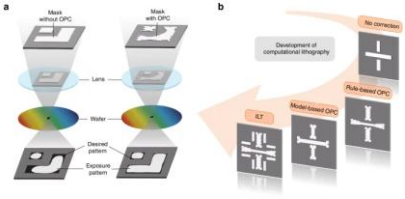
Potential roadmap extension

	2018	2020	2022	2024	2026	2028	2030	2032	2034	2036
	N7	N5	N3	N2	A14	A10	A7	A5	A3	A2
Continued dimensional scaling										
Metal pitch [nm]	40	28	22	21	18	16	16-14	16-12	16-12	16-12
Device and material innovations										
Metal tracks	7	6	6	6	5	5	5	4	<4	<4
	FinFET	FinFET	FinFET	GAA Nanosheet	GAA Nanosheet	GAA Forksheet	GAA Forksheet	CFET	CFET	CFET Atomic
Context-aware interconnect										

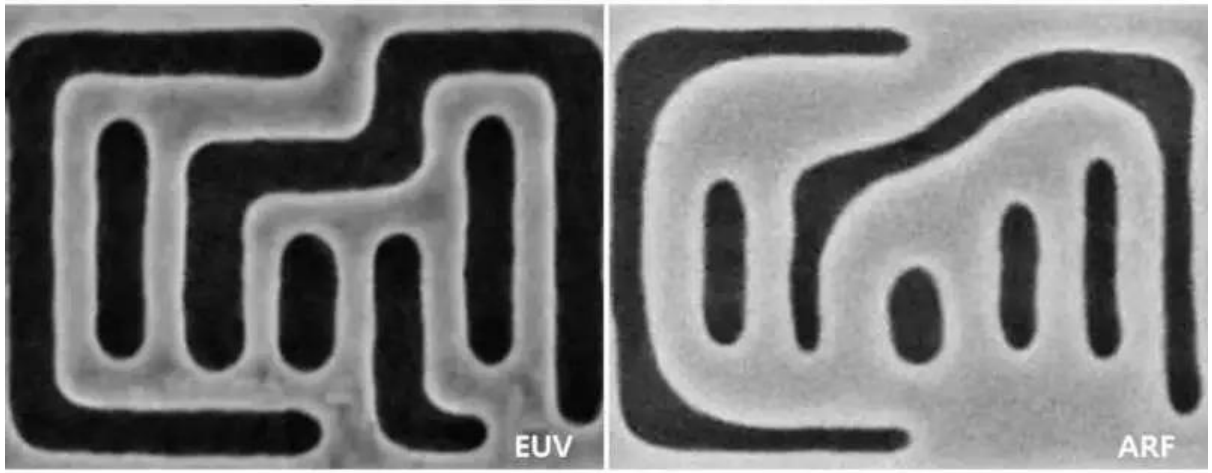


Semiconductor Process Flow





New type of Etching



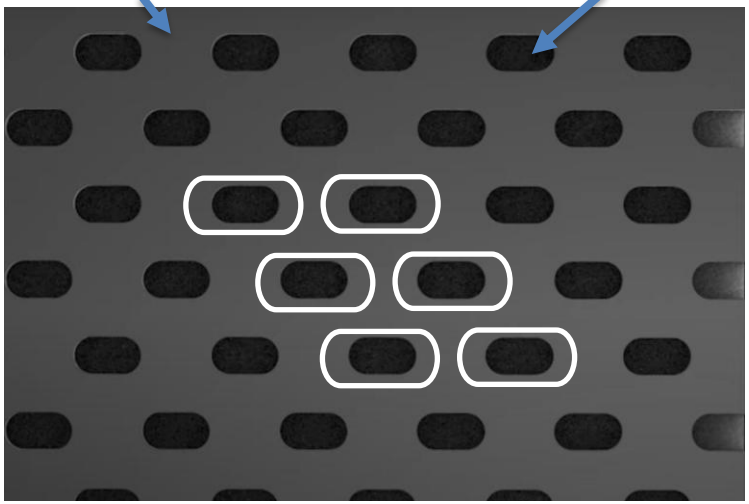
EUV limitation

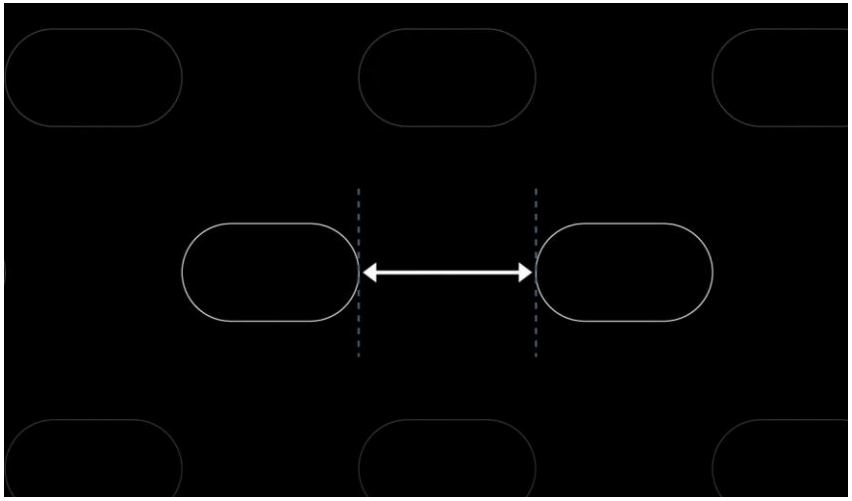
1. Uncertainty in the pattern
2. Bad line width roughness
3. Scumming at the bottom of open area
4. Large gap between patterns

SAMSUNG

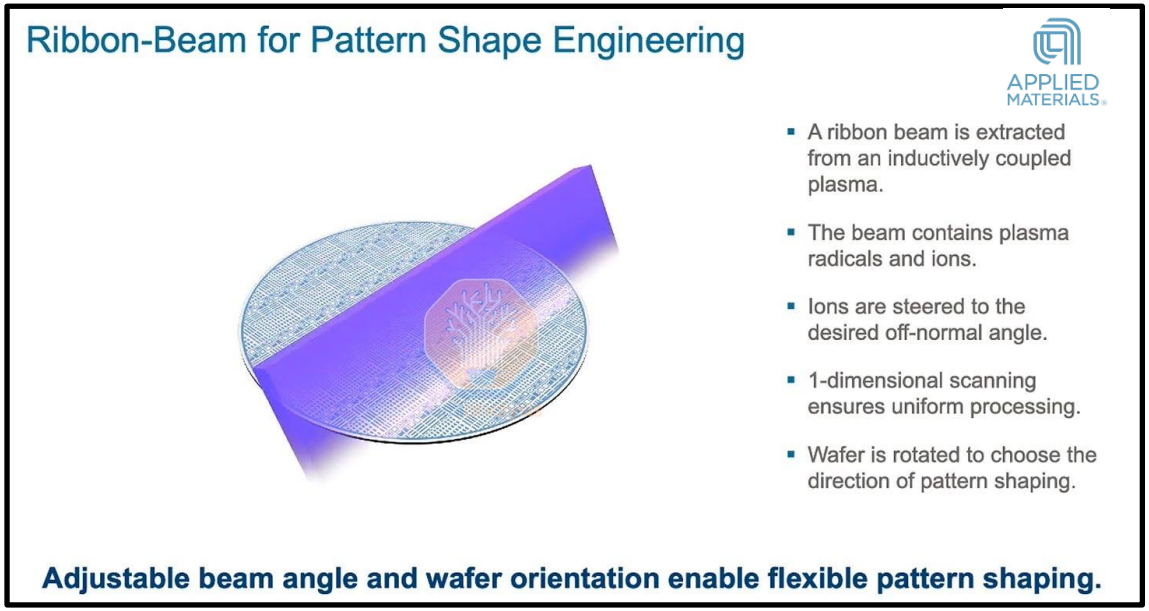
Dielectric material

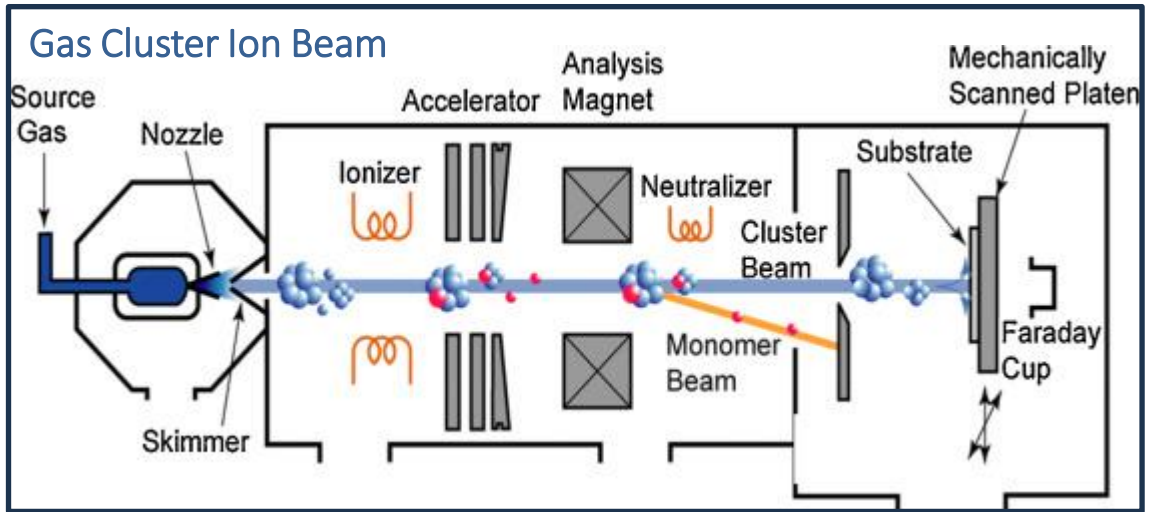
Metal area





New type of Etching





In both methods,

1. Doing directional etching
2. The Angle of the wafer and the plasma or ion beam is adjusted to the desired direction.

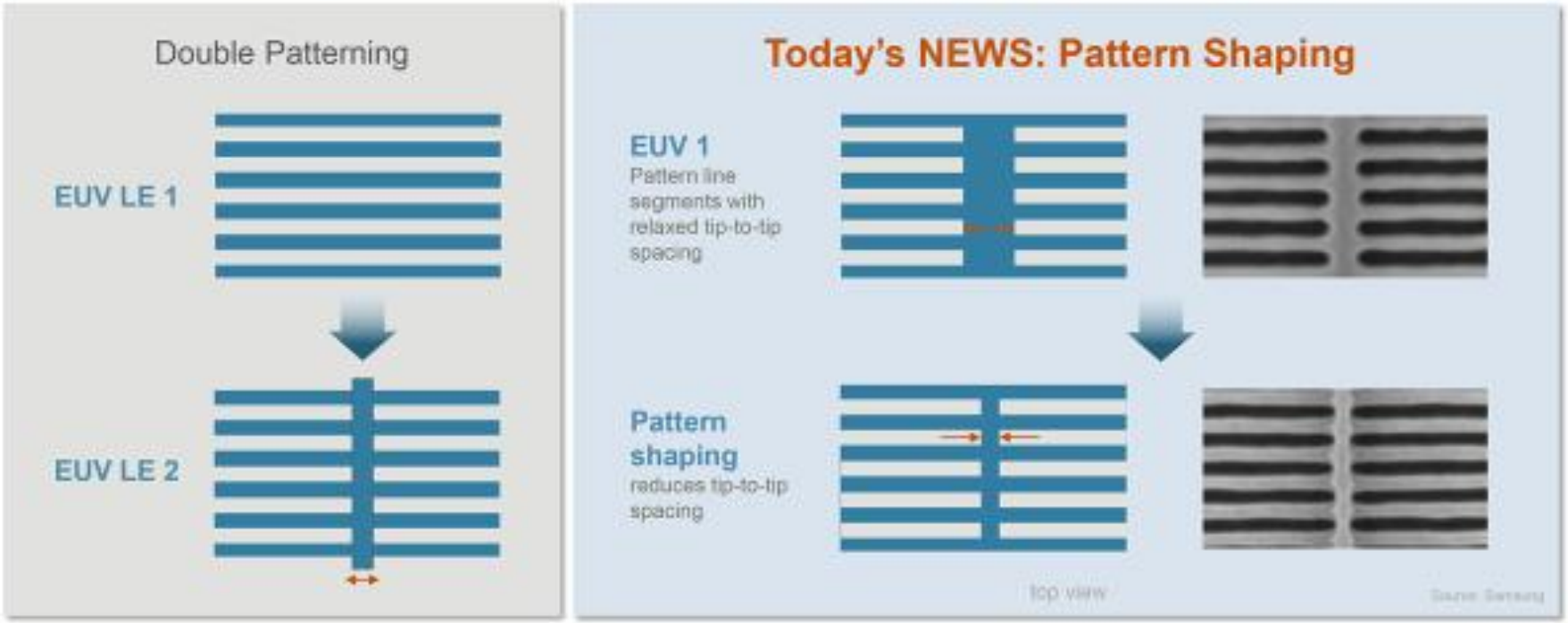
The difference between two methods,

1. Shape of Beam (Line vs Dot)
2. Scan speed

Applied Surface Science
Volume 310, 15 August 2014, Pages 77-88

New type of Etching

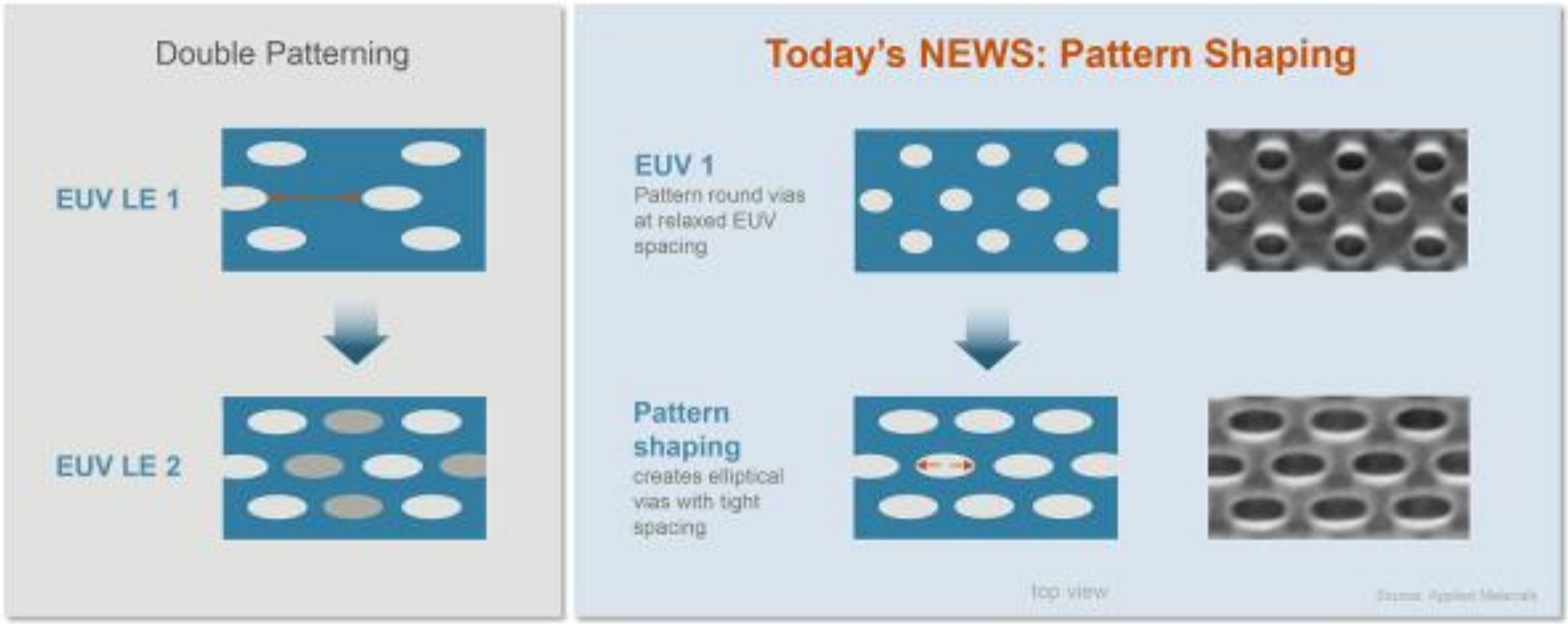
Pattern Shaping Alternative to EUV Double Patterning: Interconnect Lines



PPACt benefit: delivers the density of EUV double patterning with only one EUV step, simplifying the patterning process flow and optimizing chip area and cost

New type of Etching

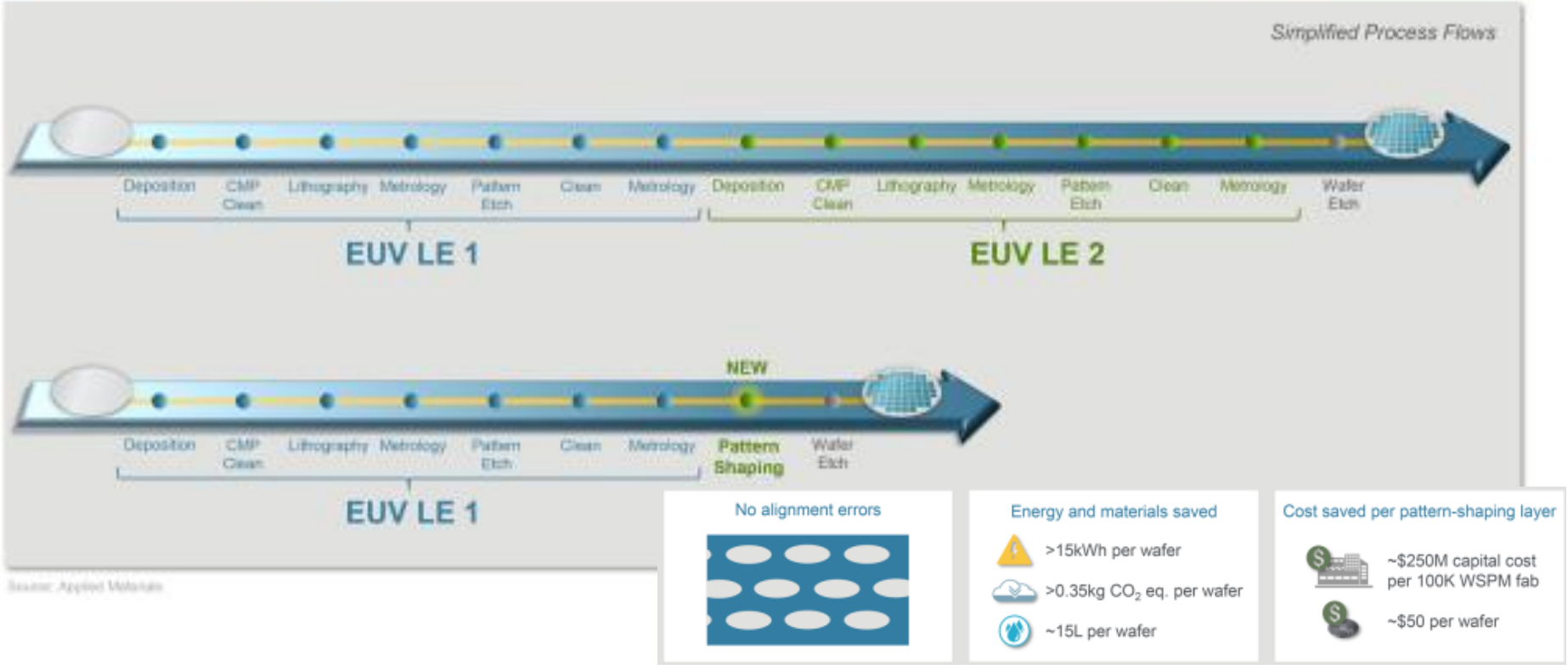
Pattern-Shaping Alternative to EUV Double Patterning: Vias



PPACt benefit: delivers high-density elliptical vias with only one EUV step, simplifying the patterning process flow – and optimizing chip power, performance, area and cost

New type of Etching

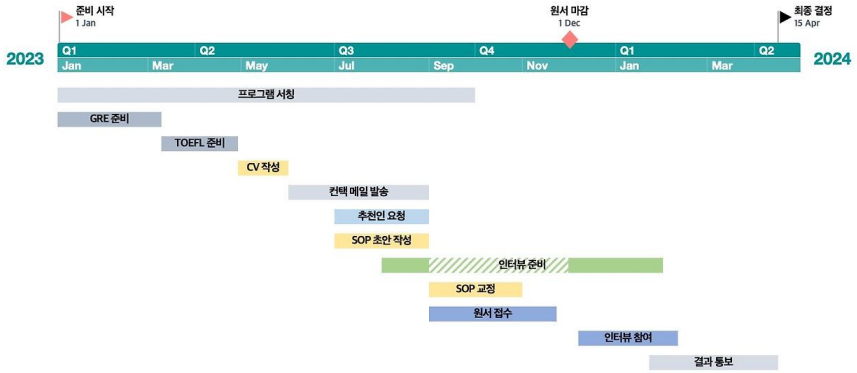
Pattern-Shaping Process Flow



Pattern shaping replaces one EUV LE process loop,
saving design and process complexity, time, energy, materials usage and cost

미국 유학 및 미국 취업

미국 박사 유학 준비: GPA, 논문(있으면 좋고, 좋은 논문 있으면 더 좋고), 영어 성적 (컴퓨터와 인사), The Graduate Record Examination (GRE), A Statemen 미국 비자 신청, 비행기 값, 1달치 생활비, 비자



미국 취업 준비: GPA, 논문(있으면 좋고), 인맥, 영어

미국 생활 준비: 비자, 영주권 (회사 서포트 or 논문

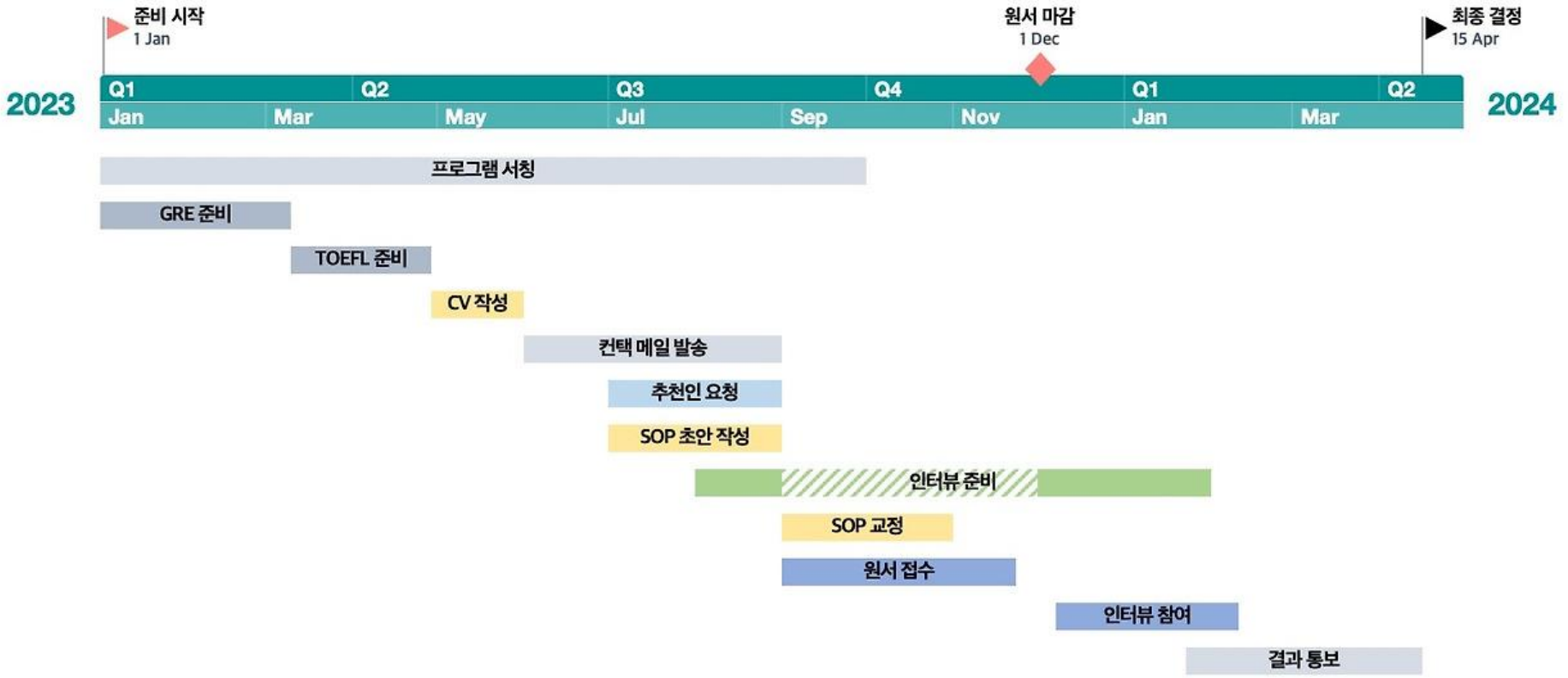
미국 생활 장점: 여유로운 삶, 노후를 위한 체계적인 시스템, 덜 치열한 사회 분위기, 어디를 가던 나에게는 새로운 여행지

미국 생활 단점: 부모님, 한국에 대한 그리움, 언어 장벽으로 인한 문제점

kjung003@ucr.edu

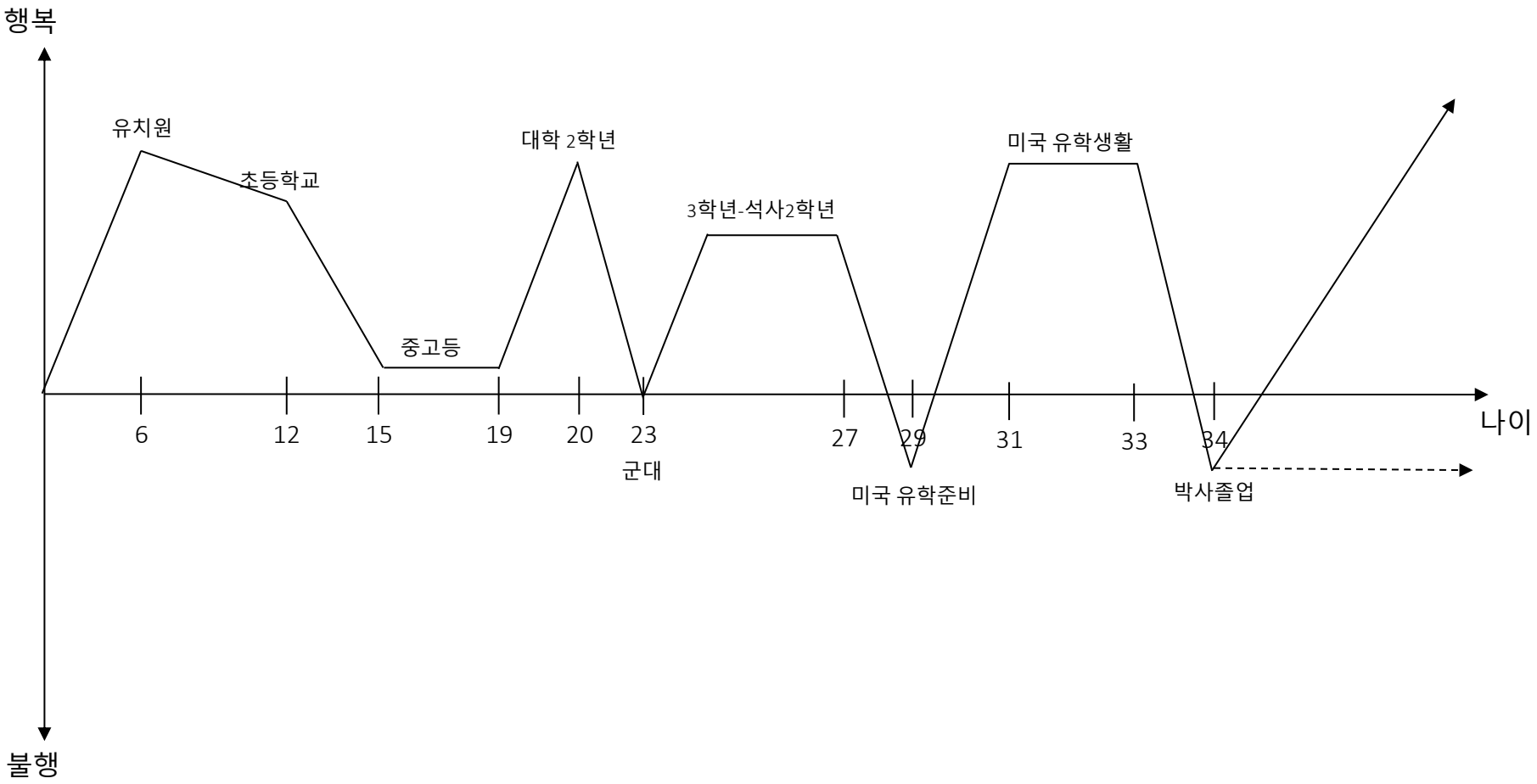
미국 유학 및 미국 취업

미국 박사` 유학 준비: GPA, 논문(있으면 좋고, 좋은 논문 있으면 더 좋고), 영어 성적 (커트라인 이상), The Graduate Record Examination (GRE), A Statement of Purpose (SOP), 미국 지도 교수 컨택, 원서비, 미국 비자 신청, 비행기 값, 1달치 생활비, 비자



https://brunch.co.kr/@kyleseling/65

나는 누구인가?


행복
유치원
초등학교
중고등
대학 2학년
3학년-석사2학년
군대
미국 유학준비
미국 유학생활
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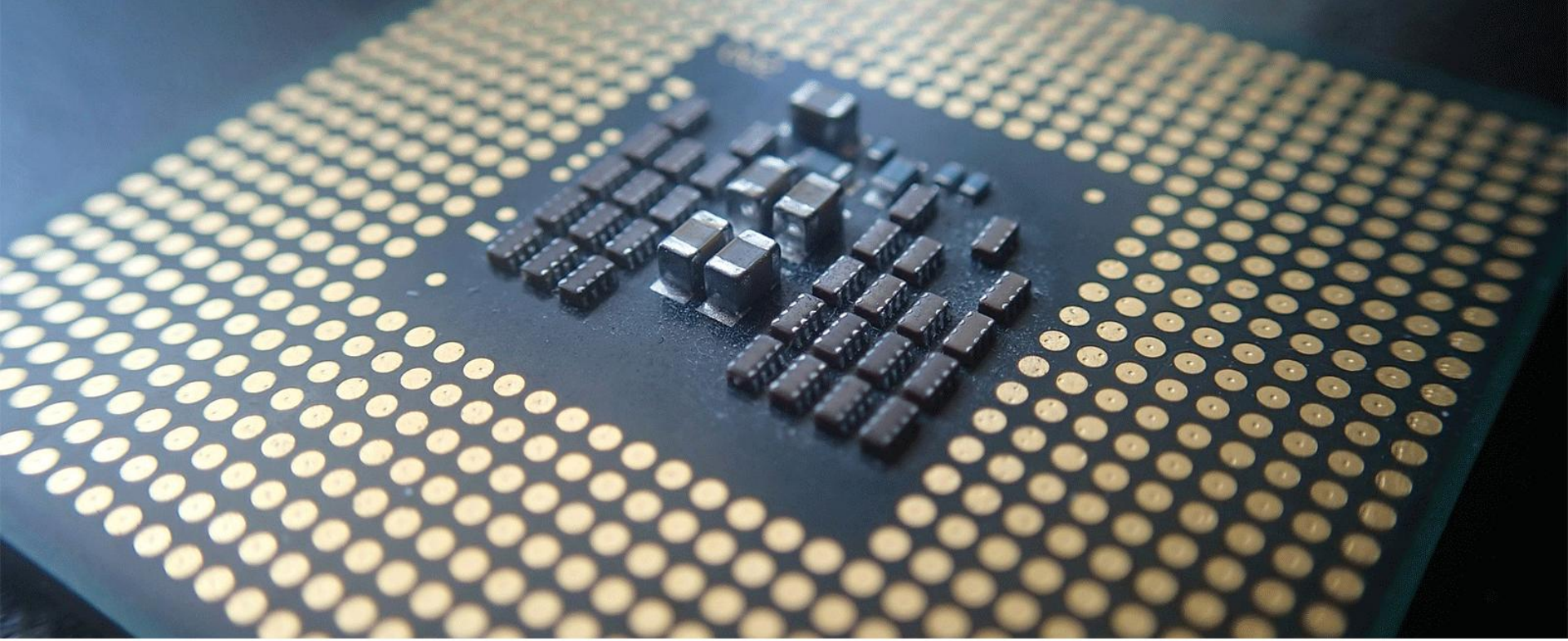
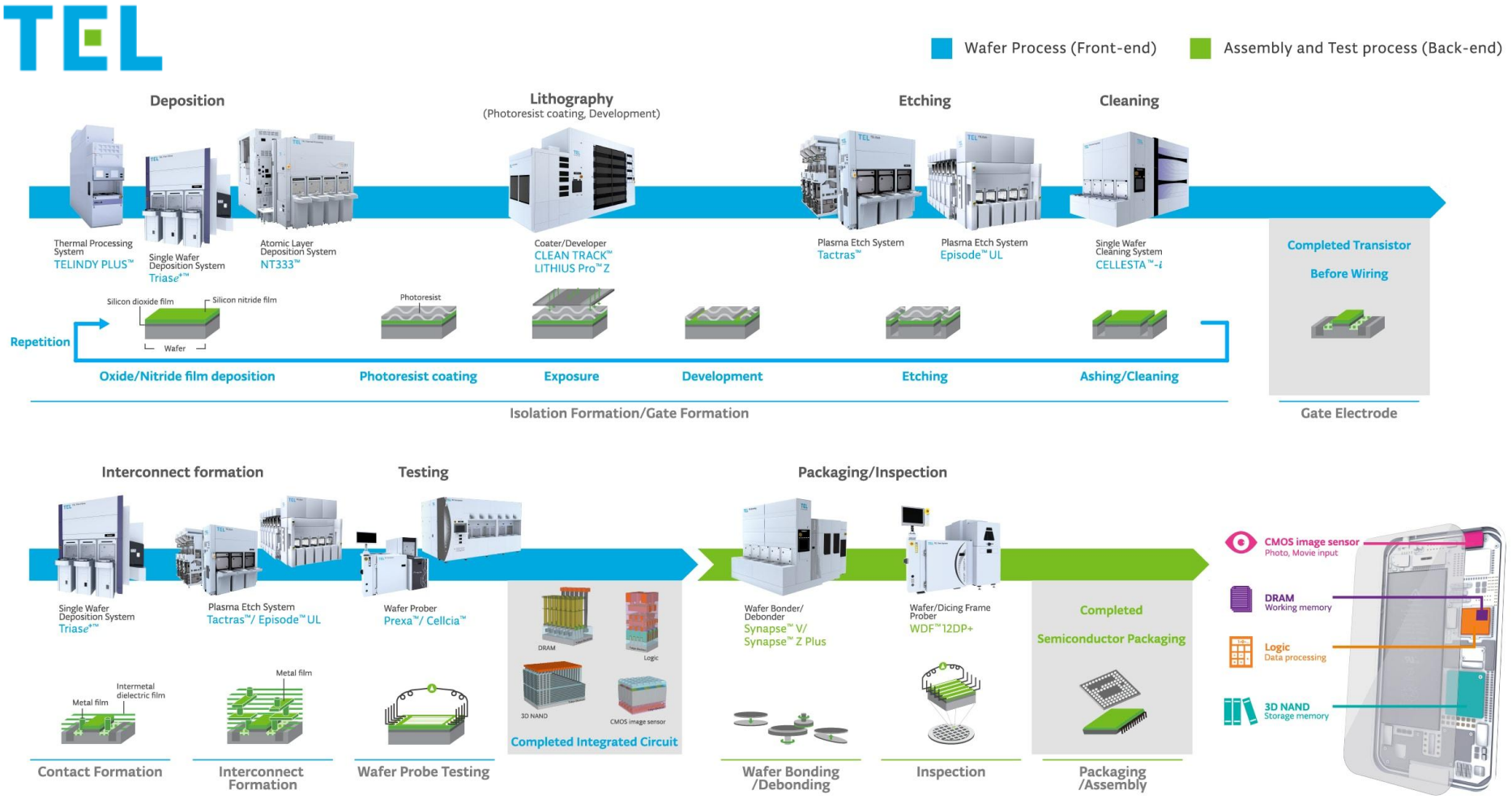
나이
불행



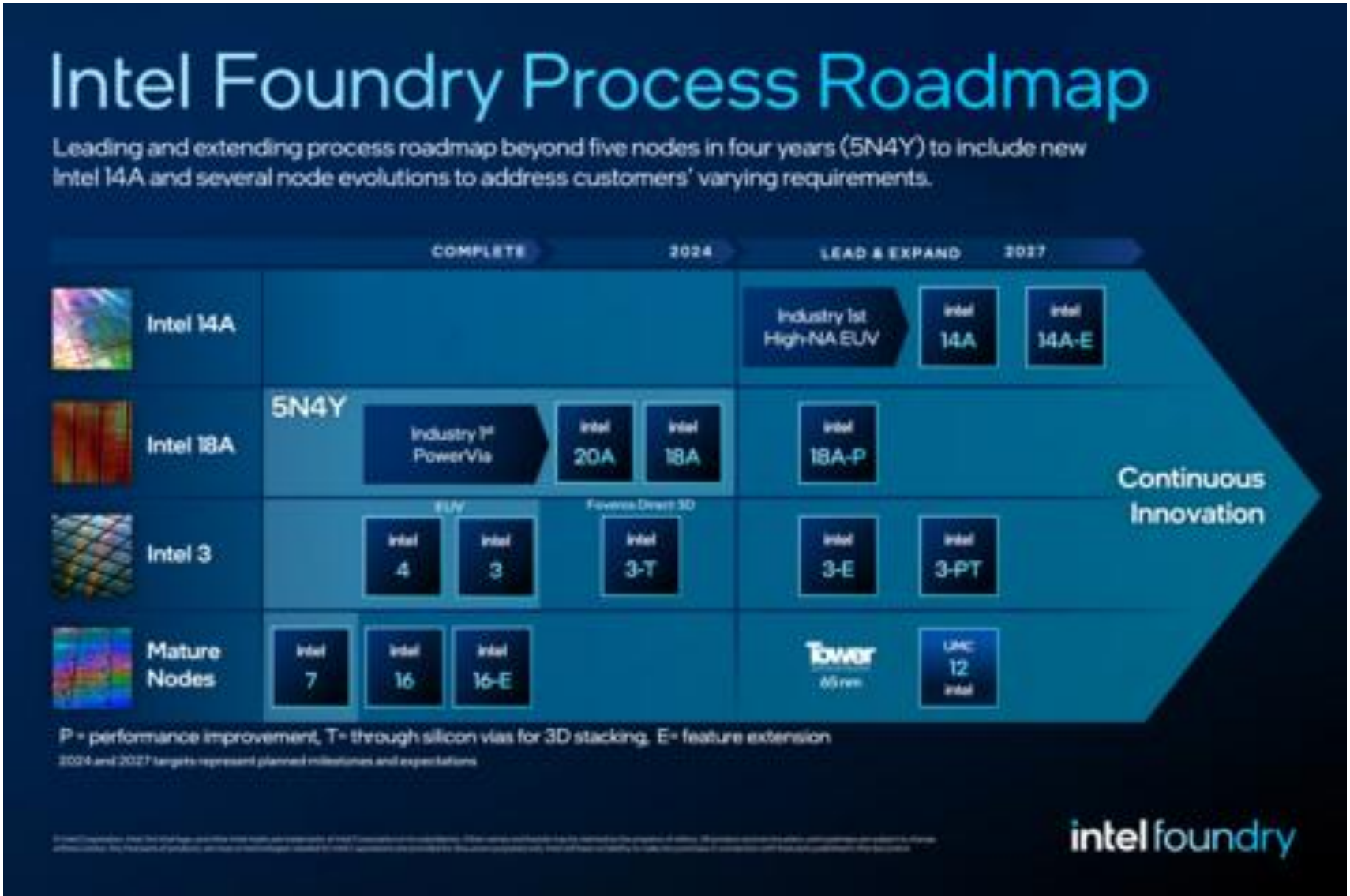
kjung003@ucr.edu

THANK YOU

업무소개

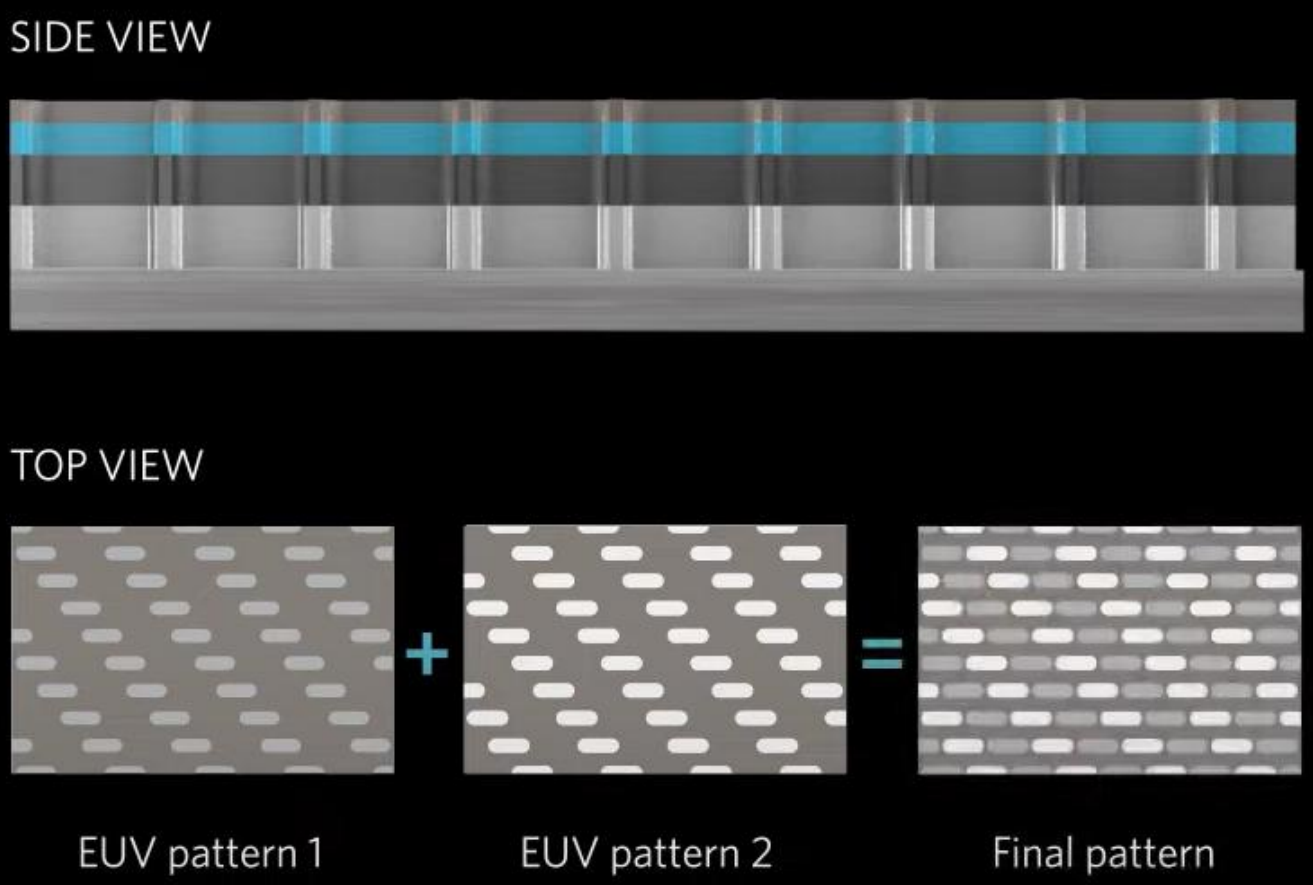

Wafer Process (Front-end)
Assembly and Test process (Back-end)
Deposition
Lithography
(Photoresist coating, Development)
Etching
Cleaning
Thermal Processing System
TELINDY PLUS™
Single Wafer Deposition System
Triase+™
Atomic Layer Deposition System
NT333™
Coater/Developer
CLEAN TRACK™
LITHIUS Pro™ Z
Plasma Etch System
Tactras™
Plasma Etch System
Episode™ UL
Single Wafer Cleaning System
CELLESTA™-i
Completed Transistor
Before Wiring
Silicon dioxide film
Silicon nitride film
Wafer
Photoresist
Repetition
Oxide/Nitride film deposition
Photoresist coating
Exposure
Development
Etching
Ashing/Cleaning
Isolation Formation/Gate Formation
Gate Electrode
Interconnect formation
Testing
Packaging/Inspection
Single Wafer Deposition System
Triase+™
Plasma Etch System
Tactras™/ Episode™ UL
Wafer Prober
Prexa™/ Cellcia™
DRAM
Logic
3D NAND
CMOS image sensor
Completed Integrated Circuit
Wafer Bonder/ Debonder
Synapse™ V/
Synapse™ Z Plus
Wafer/Dicing Frame Prober
WDF™ 12DP+
Completed
Semiconductor Packaging
Metal film
Intermetal dielectric film
Metal film
Contact Formation
Interconnect Formation
Wafer Probe Testing
Wafer Bonding /Debonding
Inspection
Packaging /Assembly
CMOS image sensor
Photo, Movie input
DRAM
Working memory
Logic
Data processing
3D NAND
Storage memory

회사소개


Intel Foundry Process Roadmap
Leading and extending process roadmap beyond five nodes in four years (5N4Y) to include new Intel 14A and several node evolutions to address customers' varying requirements.
COMPLETE
2024
LEAD & EXPAND
2027
Intel 14A
Industry 1st High-NA EUV
intel 14A
intel 14A-E
Intel 18A
5N4Y
Industry 1st PowerVia
intel 20A
intel 18A
intel 18A-P
Intel 3
EUV
Foveros Direct 3D
intel 4
intel 3
intel 3-T
intel 3-E
intel 3-PT
Mature Nodes
intel 7
intel 16
intel 16-E
Tower 65 nm
UMC 12 intel
Continuous Innovation
P = performance improvement, T= through silicon vias for 3D stacking, E= feature extension
2024 and 2027 targets represent planned milestones and expectations
intel foundry

New type of Etching

Previous approach



Semiconductor Roadmap

IMEC & ASML